AMENDMENTS TO THE SPECIFICATION

Page 6, paragraph 3:

Figure 2 illustrates diagrammatically the arrangement of the array of radiation sensitive detector elements 42 and two chips 48 which comprise 64 groups of electronic read-out circuits each, said read-out circuits comprising the charge amplifiers which are connected to the detector elements. Each of said electronic read-out circuits also includes bandpass filters and signal level comparators; an output multiplexer is also connected to the output of each of the chips in order to limit the number of output pins of the chip.

Page 10, paragraph 3:

The Figs. 6a and 6b show a logic gate in the CMOS logic and a logic gate in the CML technique, respectively. The logic gate shown in Fig. 6a consists of two MOSFET transistors 118 and 120 which are connected in series by way of their main current path, the junction 122 constituting the output for the logic signal. In the case of a transition from a logic state to the complementary logic state there will be a reactive current to the substrate. This current is produced as follows. In the first logic state of the gate a current is conducted through the output 122 which is directed inwards; in the complementary logic state a current is conducted through the output 122 which is directed outwards. In the latter case the current flows from the supply point 124 and through the transistor 118 to the output 122, so that the transistor 120 is not conductive and hence no current flows to the substrate. In the former case the current flows from the output 122 and through the transistor 120 to the substrate, so that the transistor 120 is [not] conductive. In that case a current does flow to the substrate. Upon transition of the logic state, therefore, a current difference occurs in the form of a pulse-shaped peak current or reactive current. Because the charge amplifiers constructed in the bipolar technique are also provided on the same substrate, this pulse-shaped peak current will contribute to the noise of the charge amplifiers; this would degrade the signal-to-noise ratio thereof.

Page 11, paragraph 1:

The described problem is solved by using a logic gate which is constructed in the form of CML logic as shown in Fig. 6b. This gate consists of two parallel branches 126 and 128 which are connected in series with a current source 138. Each of the two parallel branches

126 and 128 consists of a MOSFET transistor 130, 132 and a current source 134, 136, respectively. The output of this gate is formed by the two junctions [138] 139 and 140; the difference voltage between these two junctions represent the logic value. In the case of a transition between two logic states, the current decrease in one transistor, for example the transistor 130, equals the current increase in the other transistor 132 and vice versa. The substrate current is the sum of these two currents and does not change. Consequently, the undesirable pulse-shaped peak current will not occur so that it cannot make a noise contribution in the analog processing chain on the substrate.